In the Specification:

Please amend the paragraph starting on page 10, line 15, as follows:

Figure 1A shows an exemplary 128-bit VLIW packet 102 having bits 0 through 127. The length of a VLIW packet (also referred to as a "composite packet" in the present application) varies from processor to processor and may be 64 bits, 128 bits (which is the length of the VLIW packet in the present example), 256 bits or even greater. However, a common denominator in a VLIW packet is the fact that there are a number of instructions in the VLIW packet, as well as a "VLIW template" (or simply a "template"). For example, a 128-bit VLIW packet may be divided into its constituent instructions and a template in a number of ways. A 128-bit VLIW packet may consist of ~~five16-bit~~ five_16-bit instructions, one 32-bit instruction, and a 16-bit template. As another example, a 128-bit VLIW packet may consist of three 16-bit instructions, two 32-bit instructions, and a 16-bit template. In the example used in the present application, a 128-bit VLIW packet consists of three 41-bit instructions and a 5-bit template.